EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	55234	port.clm.	US-PGPUB	OR	ON	2007/02/12 09:24
L2	11376	lid.clm.	US-PGPUB	OR	ON	2007/02/12 09:24
L3	61	"local identifier".clm.	US-PGPUB	OR	ON	2007/02/12 09:25
L4	10	1 and 2 and 3	US-PGPUB	OR	ON	2007/02/12 09:28
L5	2407037	local unique individual personal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:28
L6	4222499	id identifier number code	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:29
L7	292176	5 near5 6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:29
L8	942533	port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:30
L9	76704	7 and 8	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:30
L10	10480	7 same 8	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:30
L11	11594481	@ad<"20010510"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:30
L12	5050	10 and 11	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:30
L13	148208	"709"/$.ccls. "370"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:31
L14	1993	12 and 13	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:31

L15	16670	intel.as.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:31
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L19	247963	17 and table$	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:42
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L25	323	switch$3 and 24	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:45
L26	580483	709/238, "239", "241", "235", "231".ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:45

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L27	87659	"709"/("238" "239" "241" "235" "231").ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:46
L28	2916	709/238.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:46
L29	764	709/239.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:46
L30	308	709/241.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:46
L31	641	709/235.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:46
L32	1916	709/231.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:46
L33	2814	370/229.ccls. 370/231.ccls. 370/237.ccls. 370/238.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:47
L34	8560	28 29 30 31 32 33	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/02/12 09:47
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1 Papers: A review of port scanning techniques
◆ Marco de Vivo, Eddy Carrasco, Germinal Isern, Gabriela O. de Vivo
 April 1999 **ACM SIGCOMM Computer Communication Review**, Volume 29 Issue 2
 Publisher: ACM Press
 Full text available: 📄 pdf(661.44 KB)   Additional Information: full citation, abstract, references, citings

 This paper reports the most important techniques used by **TCP port scanners**. TCP port
 scanners are specialized programs used to determine what TCP ports of a host have
 processes *listening on* them for possible connections. Since these ports characterize, in
 part, the amount of exposure of the hosts to potential external attacks, knowing their
 existence is a fundamental matter for network and/or security administrators. Moreover,
 as scanners are also used by hackers, administra ...

 Keywords: Coordinated Scanning, Decoy Scanning, FIN Scanning, Fingerprinting,
 Indirect Scanning, SYN Scanning, Stealth Scanning, TCP/IP, Three-way Handshake, UDP

2 The PORT Mathematical Subroutine Library
◆ P. A. Fox, A. P. Hall, N. L. Schryer
 June 1978 **ACM Transactions on Mathematical Software (TOMS)**, Volume 4 Issue 2
 Publisher: ACM Press
 Full text available: 📄 pdf(1.60 MB)   Additional Information: full citation, references, citings, index terms

3 Heterogeneous technology mapping for FPGAs with dual-port embedded memory
◆ **arrays**
 Steven J. E. Wilton
 February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium
                on Field programmable gate arrays FPGA '00**
 Publisher: ACM Press
 Full text available: 📄 pdf(597.01 KB)   Additional Information: full citation, abstract, references, citings, index terms

 It has become clear that on-chip storage is an essential component of high-density
 FPGAs. These arrays were originally intended to implement storage, but recent work has
 shown that they can also be used to implement logic very efficiently. This previous work
 has only considered single-port arrays. Many current FPGAs, however, contain dual-port
 arrays. In this paper we present an algorithm that maps logic to these dual-port arrays.
 Our algorithm can either optimize area with no regar ...

4 <u>Architectural walkthroughs using portal textures</u>
Daniel G. Aliaga, Anselmo A. Lastra
October 1997 **Proceedings of the 8th conference on Visualization '97 VIS '97**
Publisher: IEEE Computer Society Press
Full text available: <u>pdf(980.76 KB)</u>
<u>Publisher Site</u>
Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

5 <u>A study on the number of memory ports in multiple instruction issue machines</u>
Soo-Mook Moon, Kemal Ebcioğlu
December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture MICRO 26**
Publisher: IEEE Computer Society Press
Full text available: <u>pdf(1.28 MB)</u>   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>

Keywords: ILP, memory disambiguation, memory ports, speculative loads, static scheduling

6 <u>Increasing cache port efficiency for dynamic superscalar microprocessors</u>
Kenneth M. Wilson, Kunle Olukotun, Mendel Rosenblum
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2
Publisher: ACM Press
Full text available: <u>pdf(1.09 MB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

The memory bandwidth demands of modern microprocessors require the use of a multi-ported cache to achieve peak performance. However, multi-ported caches are costly to implement. In this paper we propose techniques for improving the bandwidth of a single cache port by using additional buffering in the processor, and by taking maximum advantage of a wider cache port. We evaluate these techniques using realistic applications that include the operating system. Our techniques using a single-ported ca ...

7 <u>Synchronization for a multi-port frame buffer on a mesh-connected multicomputer</u>
Bin Wei, Gordon Stoll, Douglas W. Clark, Edward W. Felten, Kai Li, Patrick Hanrahan
December 1995 **Proceedings of the IEEE symposium on Parallel rendering PRS '95**
Publisher: ACM Press
Full text available: <u>pdf(856.27 KB)</u>   Additional Information: <u>full citation</u>, <u>citings</u>, <u>index terms</u>

Keywords: mesh routing network, multi-port frame buffer, multicomputers, parallel rendering, synchronization

8 <u>Optimal privacy and authentication on a portable communications system</u>
Ulf Carlsen
July 1994 **ACM SIGOPS Operating Systems Review**, Volume 28 Issue 3
Publisher: ACM Press
Full text available: <u>pdf(699.70 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>citings</u>, <u>index terms</u>

Beller, Chang and Yacobi [2] have recently proposed a set of secret key and public key protocols to meet authentication and privacy requirements for conversation set-up protocols for the initiating party of portable communication systems. This paper improves upon the protocols to obtain a higher assurance of authentication and key distribution.

Conversation set-up protocols for the responding party are discussed, a public key protocol providing end-to-end authentication and privacy is described, ...

9 Port activity simulation: an overview
Said Ali Hassan
December 1993 **ACM SIGSIM Simulation Digest,** Volume 23 Issue 2
Publisher: ACM Press
Full text available: pdf(1.22 MB)   Additional Information: full citation, abstract, references, index terms

Port can be viewed as a complex system containing several entities with interfering attributes. The whole image is very complex and special care should be considered to model such systems.Several works for investigating, analysing evaluating and improving port activities are carried out, each of them is concerned with a specific area related to the port functions, the key tool for most of these works is the simulation.The purpose of this paper is to give an overview of a computer simulation prog ...

10 A three-port/three-access register file for concurrent processing and I/O communication in a RISC-like graphics engine
M. L. Anido, D. J. Allerton, E. J. Zaluska
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture ISCA '89,** Volume 17 Issue 3
Publisher: ACM Press
Full text available: pdf(708.55 KB)   Additional Information: full citation, abstract, references, citings, index terms

A novel method that provides extremely fast Input/Output (I/O) data transfer to a RISC-like graphics engine is presented. This method employs a combined two-port / two-access and a three-port / three-access register file used for concurrent processing and I/O data transfer. The three-port cell employed is only 25 % larger than the two-port cell, offering considerable advantages over alternative approaches, such as FIFOs or register banks. This paper discusses some methods that ca ...

11 Port calling: a transformation for reducing I/O during multi-package functional partitioning
Frank Vahid
September 1997 **Proceedings of the 10th international symposium on System synthesis ISSS '97**
Publisher: IEEE Computer Society
Full text available: pdf(795.56 KB)
Publisher Site   Additional Information: full citation, abstract, references, citings

Partitioning a system among multiple input and output pin (I/O) limited packages is a widely researched and hard to solve problem. We previously described a new approach yielding large improvements, which partitioned functions rather than structure, and which used a single bus for all inter-package data transfer. In this paper, we describe an extension permitting arbitrary distribution of I/O among the packages, and highlight experiments demonstrating even further I/O reductions as well as surpr ...

Keywords: Functional partitioning, hardware/software codesign, system synthesis, communication, transformation

12 Thoth, a portable real-time operating system
David R. Cheriton, Michael A. Malcolm, Lawrence S. Melen, Gary R. Sager
February 1979 **Communications of the ACM,** Volume 22 Issue 2
Publisher: ACM Press
Full text available: pdf(1.23 MB)   Additional Information: full citation, abstract, references, citings

Thoth is a real-time operating system which is designed to be portable over a large set of

machines. It is currently running on two minicomputers with quite different architectures. Both the system and application programs which use it are written in a high-level language. Because the system is implemented by the same software on different hardware, it has the same interface to user programs. Hence, application programs which use Thoth are highly portable. Thoth encourages structuring progr ...

Keywords: minicomputer, operating systems, portability, real time

13 Reality portals

Karl-Petter Åkesson, Kristian Simsarian
December 1999 **Proceedings of the ACM symposium on Virtual reality software and technology VRST '99**
Publisher: ACM Press
Full text available: 📄 pdf(1.58 MB)   Additional Information: full citation, abstract, references, index terms

Through interactive augmented virtuality we provide the ability to interactively explore a remote space inside a virtual environment. This paper presents a tool and technique that can be used to create such virtual worlds that are augmented by video textures taken of real world objects. The system constructs and updates, in near real-time, a representation of the user-defined salient and relevant features of the real world. This technique has the advantage of constructing a virtual world th ...

Keywords: augmented virtuality, collborative virtual environments, environment visualization, teleoperation, video textures

14 Learning binary matroid ports

Lisa Hellerstein, Collette Coullard
January 1994 **Proceedings of the fifth annual ACM-SIAM symposium on Discrete algorithms SODA '94**
Publisher: Society for Industrial and Applied Mathematics
Full text available: 📄 pdf(904.16 KB)   Additional Information: full citation, references, index terms

15 Two-ported cache alternatives for superscalar processors

Andrew Wolfe, Rodney Boleyn
December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture MICRO 26**
Publisher: IEEE Computer Society Press
Full text available: 📄 pdf(1.01 MB)   Additional Information: full citation, references, citings

16 Register file port requirements of transport triggered architectures

Jan Hoogerbrugge, Henk Corporaal
November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture MICRO 27**
Publisher: ACM Press
Full text available: 📄 pdf(533.24 KB)   Additional Information: full citation, abstract, references, citings, index terms

Exploitation of large amounts of instruction level parallelism requires a large amount of connectivity between the shared register file and the function units; this connectivity is expensive and increases the cycle time.This paper shows that the new class of transport triggered architectures requires fewer ports on the shared register file than traditional operation triggered architectures. This is achieved by programming data-transports instead of operations.Experimen ...

17 Dynabook revisited—portable computers past, present and future

Larry Press
March 1992 **Communications of the ACM**, Volume 35 Issue 3
Publisher: ACM Press
Full text available: pdf(2.18 MB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

18 <u>New life in dusty decks: results of porting a CM Fortran based aeroacoustic model to high performance Fortran</u>
Jeffrey J. Nucciarone, Yusuf Özyörük, Lyle N. Long
November 1997 **Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '97**
Publisher: ACM Press
Full text available: pdf(110.48 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>

The High Performance Fortran language is a 'standard by consensus', developed by individuals and vendors in the high performance computing industry, to provide a low barrier entry to parallel computing. It promises to be an easier to use development environment for distributed memory computing platforms compared to the programming complexity required by message passing libraries such as PVM and MPI. HPF promises much and is still in its infancy.Since HPF was developed in part based on experience ...

Keywords: Thinking Machines CM Fortran, aeroacoustics, dusty decks, high performance Fortran

19 <u>Portals and mirrors: simple, fast evaluation of potentially visible sets</u>
David Luebke, Chris Georges
April 1995 **Proceedings of the 1995 symposium on Interactive 3D graphics SI3D '95**
Publisher: ACM Press
Full text available: pdf(4.39 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

We describe an approach for determining potentially visible sets in dynamic architectural models. Our scheme divides the models into cells and portals, computing a conservative estimate of which cells are visible at render time. The technique is simple to implement and can be easily integrated into existing systems, providing increased interactive performance on large architectural models.

20 <u>Saving portable computer battery power through remote process execution</u>
Alexey Rudenko, Peter Reiher, Gerald J. Popek, Geoffrey H. Kuenning
January 1998 **ACM SIGMOBILE Mobile Computing and Communications Review**, Volume 2 Issue 1
Publisher: ACM Press
Full text available: pdf(1.28 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>

We describe a new approach to power saving and battery life extension on an untethered laptop through wireless remote processing of power-costly tasks. We ran a series of experiments comparing the power consumption of processes run locally with that of the same processes run remotely. We examined the trade-off between communication power expenditures and the power cost of local processing. This paper describes our methodology and results of our experiments. We suggest ways to further improve thi ...

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CNF = IEE Conference,   IEEE STD = IEEE Standard

1. **A Programmable Preprocessor for Parallelizing Fortran-90**
   Rosing, M.; Yabusaki, S.;
   Supercomputing, ACM/IEEE 1999 Conference
   13-18 Nov. 1999 Page(s):3 - 3
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2. **New Life in Dusty Decks: Results of Porting a CM Fortran Based Aeroacoustic Model to High Performance
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   Nucciarone, J.J.; Ozyoruk, Y.; Long, L.N.;
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   Ding, J.; Sobelman, G.E.;
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6. **NAS experiences of porting CM Fortran codes to HPF on IBM SP2 and SGI Power Challenge**
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   Zhongqi Jing; Smith, S.; Jain, M.; Zalrai, A.;
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8. **A method for estimating local traffic load in a simulcast radio system**
   Ariyavisitakul, S.L.; Greenstein, L.J.;
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Acosta, E.; Stephens, B.; Temkin, B.; Krummel, T.M.; Gorman, P.J.; Griswold, J.A.; Deeb, S.A.;
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Cavanagh, J.P.;
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Volume 30, Issue 3, March 1992 Page(s):48 - 54, 63-4
IEEE JNL

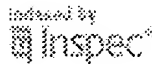12. **Multiplexing of MPEG video sources over an ATM LAN**
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13. **Statistical delay analysis with self-similar input traffic in ATM networks**
Shibin Song; Kee-Yin Ng, J.; Tang, B.;
Real-Time Computing Systems and Applications, 1999. RTCSA '99. Sixth International Conference on
13-15 Dec. 1999 Page(s):133 - 140
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